Novel Unipolar Complementary Field-Effect Transistor Technology

**OCR Number:** OCR 4977

**Description:**

Yale researchers have developed an all N-channel CMOS (Complementary Metal-Oxide-Semiconductor) technology that overcomes the problem of low hole mobility. The building block for conventional CMOS technology consists of N-channel (electron) and P-channel (hole) MOSFETs. However, electron mobility is much greater than hole mobility in semiconductors, with the ratio of electron:hole mobility ranging from 2.8 in silicon to >80 in indium arsenide. Yale’s novel technology utilizes the double channel capability of a MOSFET built with a SOI (semiconductor on insulator) structure to eliminate P-channels and replace them with N-channels, resulting in increased switching speed. This technology can be implemented with both silicon and III-V semiconductors.

**Advantages:** In addition to increased switching speed, this technology is simpler to fabricate than conventional CMOS, as it requires fewer materials and does not require P-well and N-well isolation. Furthermore, the technology allows for higher device density on a chip (leading to reduced cost per function) because channel width does not have to be widened to compensate for reduced hole mobility.

**Field of Application:** Semiconductor devices, CMOS logic, field-effect transistors.

![Figure 1. Schematic of all n-channel CMOS](image)

**Stage of Development:** Experimental proof-of-principles in progress.
Published/Issued Patents: U.S. Patent No. 8,384,156

Licensing Contact: Richard Andersson
richard.andersson@yale.edu